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A Smart Current Modulation Scheme for Harmonic Reduction in Three-Phase Motor Drive Applications

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Keywords

«Harmonics», «Modulation strategy», «Power factor correction», «Three-phase system»

Abstract

Electric motor-driven systems consume considerable amount of the global electricity. Majority of three-phase motor drives are equipped with conventional diode rectifier and passive harmonic mitigation, being witnessed as the main source in generating input current harmonics. While many active harmonic mitigation methods have been developed over the years, the total cost and complexity has become the main obstacle in employing prior-art methods for motor drive systems. This paper presents a novel current modulation method based on the electronic inductor concept for three-phase ac-dc systems to reduce input current harmonics. The obtained results at simulation and experimental levels confirm the effectiveness of the proposed approach.

1. Introduction

Non-linear characteristics of the diode rectifier cause harmonic input current, which has undesirable consequences [1]-[6]. The problem associated with the harmonic distortion is unnecessary losses and heat in power system transformers and nuisance tripping of circuit breakers and over-stressing of power factor correction capacitors. This highlights the necessity for the drive systems to maintain the level of the generated current harmonics within the acceptable limits and recommended by standards, such as IEC61000 [7]. This problem becomes significant when a large number of industrial converters and variable speed drives are connected to a Point of Common Coupling (PCC), where other users are also connected to the same network.

As Fig. 1 illustrates, typically in a motor drive system a three-phase diode rectifier is employed as the first conversion stage following with a voltage source inverter [3], [7]. Simplicity, reliability, robustness, and being cost-effective are the main reasons that the majority of the systems apply a diode rectifier at the front-end. However, diode rectifiers impose a high level of input current harmonics. The performance can be improved by the application of passive filtering (see Fig. 1) by employing ac-side or dc-side inductance [1], [4]-[6]. Passive filters are a cost effective solution at low power (below 10 kW), but they are bulky, worsen the system dynamic and behavior, introduce resonance in a power system and their performance depends on load profile and the power system configuration. As a consequence, a vast of active harmonic mitigation methods have been introduced to improve the input current quality by reducing its low order harmonic contents [4]-[6], [8]-[11].

Recent technological progresses in power semiconductor industry have changed the perception of active methods. However cost, efficiency and power density (W/kg) are the most demanded features.

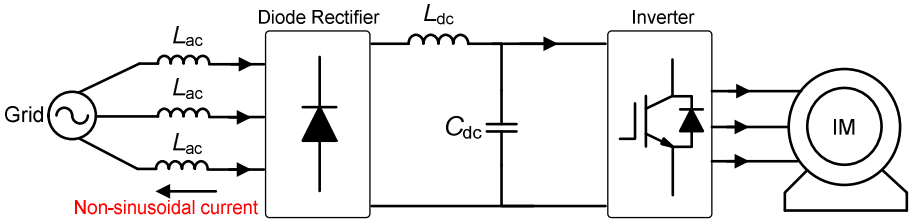


Fig. 1: A block diagram of a motor drive system.

Thus, from industry perspective, these are the key elements of success in power converters design and development. This is specially the case with the applications where there is no need to obtain a pure sinusoidal input current as long as they comply with the standard recommendation. One of these methods is employing electronic inductor suitable for low and medium power motor drive applications [4], [12]-[17].

The proposed method tackles the aforementioned challenges with an effective current modulation scheme based on the electronic inductor concept suitable for three-phase systems. Different cases have been analyzed and verified through simulation and practical experimentation.

2. Electronic Inductor

The basic idea of electronic inductor is to replace the bulky dc-side inductor with a relatively small inductor which by incorporation of a dc-dc converter it emulates the behavior of an ideal infinite inductor [12], [13], [15]. Hence, the input current will be a square-wave with 120 degrees conduction due to the fact that at each instant of time only two phases conduct and circulate dc link current through the main supply (see Fig. 2). This operating mode is a continuous conduction mode as the dc link current is always positive and never reaches to zero.

The harmonics of a line current with a square waveform can be calculated applying Fourier series analysis as follows [12]:

$$i_n = \frac{4}{n\pi} I_{dc1} \cos(n\alpha) \tag{1}$$

As Fig. 2 illustrates, for a three-phase diode rectifier, the phase angle α is 30^o while for a controlled rectifier the phase angle depends on control system and applications.

3. Proposed Current Modulation Strategy

The proposed current modulation approach is based on adding (or subtracting) phase-displaced current levels which can have certain low frequency harmonics eliminated in the three-phase input line currents. This technique is based on the calculation of a preprogrammed switching pattern for the dc-link current to obtain input currents with zero content in those specific harmonics.

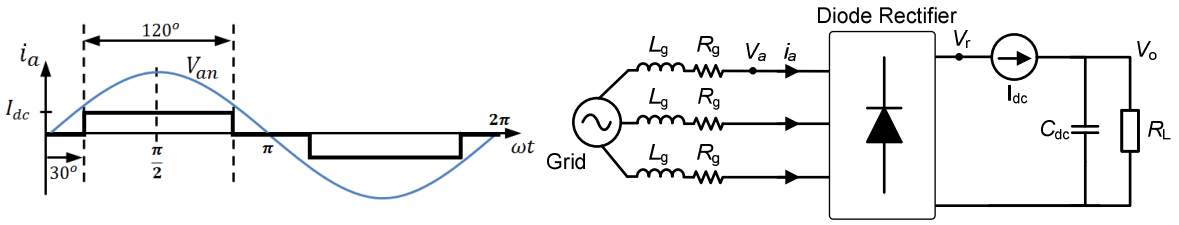


Fig. 2: A circuit diagram of a three phase diode rectifier with a constant controlled current at DC link.

Adding the new current level in a symmetrical way (see Fig. 3) results in a half-wave symmetry and having sum of the three-phase input currents to be zero at any instant of time. The first feature makes the even harmonics to disappear from the current waveform, while the latter one cancels out all tripled harmonics in a balanced system. As Fig. 3 depicted the proposed current waveform is comprises of three square-wave signals with different magnitudes and pulse widths. The first current waveform has the magnitude of I_{dc1} with the conduction phase angle of 30° which is defined based on the normal operating modes of a three-phase diode rectifier and the conduction phase angle cannot be controlled. The second current waveform has the magnitude of I_{dc2} with the conduction phase angle of α_1. The third current waveform has the magnitude of I_{dc2} but with a different conduction phase angle (α_2). These current waveforms can be analyzed based on (1) in which the fundamental input current magnitude and its harmonics can be calculated as follows:

$$i_n = \frac{4}{n\pi}[I_{dc1}\cos(n30) + I_{dc2}\cos(n\alpha_1) - I_{dc2}\cos(n\alpha_2)] \tag{2}$$

Equation (2) shows that the fundamental current can be defined by selecting the variables I_{dc1}, I_{dc2}, α_1 and α_2 but a main consequence will be on harmonic magnitudes. Therefore an optimum selection of these parameters is required to improve the quality of the input current. According to the line current waveform depicted in Fig. 3 the following condition should be valid:

$$2\beta + \theta = 60 \quad where\ \beta = \alpha_1 - 30\ and\ \theta = \alpha_2 - \alpha_1 \tag{3}$$

By substituting the conduction phase angles α_1 and α_2 in (3), the condition to satisfy waveform symmetry is as follows:

$$2\beta + \theta = 2(\alpha_1 - 30) + (\alpha_2 - \alpha_1) = 60 \quad or \quad \alpha_1 + \alpha_2 = 120 \tag{4}$$

Considering (2) and having α_1 and α_2 as the switching angles, up to two selected low order harmonics can be cancelled out. The mathematical statement of these conditions is then (e.g. $k = 5$ and $m = 13$):

$$\begin{aligned} i_1 &= \frac{4}{\pi}[I_{dc1}\cos(30) + I_{dc2}\cos(\alpha_1) - I_{dc2}\cos(\alpha_2)] \\ i_k &= \frac{4}{k\pi}[I_{dc1}\cos(k30) + I_{dc2}\cos(k\alpha_1) - I_{dc2}\cos(k\alpha_2)] = 0 \\ i_m &= \frac{4}{m\pi}[I_{dc1}\cos(m30) + I_{dc2}\cos(m\alpha_1) - I_{dc2}\cos(m\alpha_2)] = 0 \end{aligned} \tag{5}$$

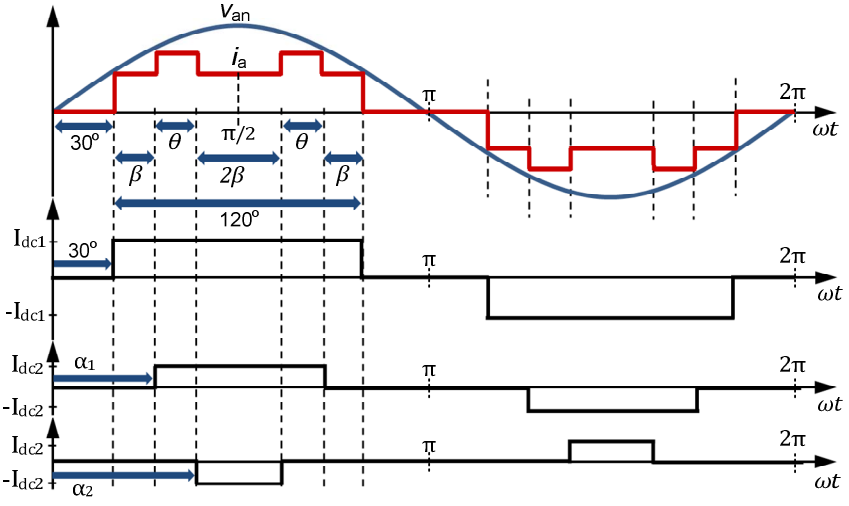


Fig. 3: Detailed analysis of the proposed current waveform with selected harmonic cancellation.

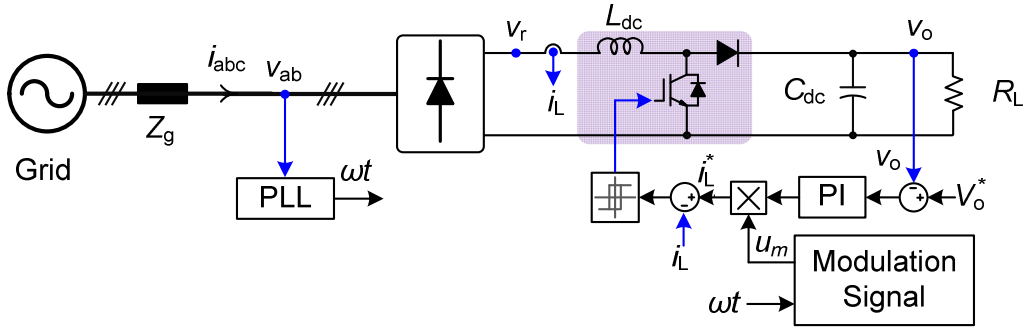
This is a system of three transcendental equations with four unknown variables I_{dc1}, I_{dc2}, α_1, α_2. Therefore, as the equations are nonlinear, mathematical methods or numerical solutions are required to find proper values for these variables to satisfy the following rule:

$$30° < \alpha_1 < 90° , \alpha_2 = 120° - \alpha_1 \quad (6)$$

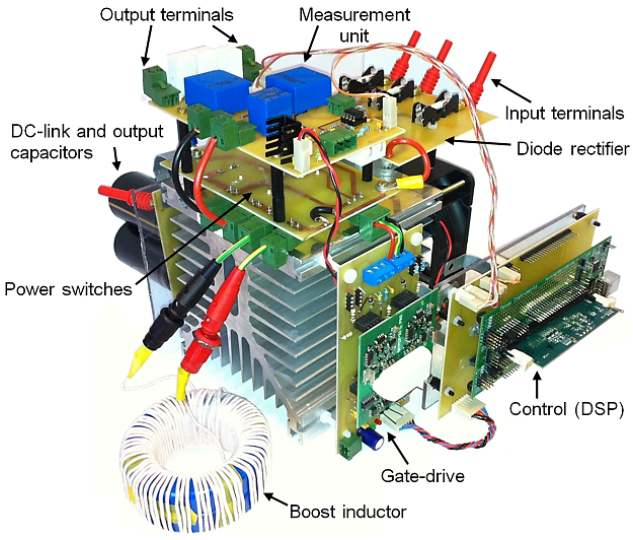
4. Single Switch Three-Phase Boost Rectifier System

Fig. 4 shows the block diagram and a photograph of the experimental hardware setup. Employing a boost converter topology, the dc link current magnitude and shape can be controlled based on the waveform shown in Fig. 3. Moreover, as the dc link current is controlled based on the load power it has the advantage of keeping the total harmonic distortion of the input current (THD_i) independent of load profile. Using the conventional boost topology also has the advantage of boosting the output dc voltage which is suitable for motor drive application since the dc link is fed to the inverter. The reference tracking performance of the current controller has an important role on harmonic mitigation, thus employing fast current control methods such as hysteresis or dead-beat are of much interest. Since in motor-driven applications the load profile is almost constant therefore employing hysteresis method will not cause a well-known variable switching frequency issue.

To synchronize the current controller with the grid a second-order generalized integrator (SOGI) based phase locked loop (PLL) system is adopted [18]. As Fig. 4 depicted, for the simplicity, the line-to-line voltage is fed to the PLL therefore the result will have 30° phase shift regarding to the phase voltage which should be corrected within the reference current generator algorithm. Here, one SKD 30 was used as a three-phase bridge rectifier and one SK60GAL125 IGBT-diode module employed in boost topology. A Texas Instrument TMS320F28335 used for control purpose and LEM current and voltage transducers are used in the measurement unit.



(a)



(b)

Fig. 4: The Implemented three-phase ac-dc system with proposed selective harmonic elimination method, (a) circuit block diagram, and (b) photograph of the hardware setup.

5. Simulation Results

In this section, simulations have been conducted to verify the effectiveness of the proposed current modulation scheme. The transcendental equations have been solved using a MATLAB function – "fsolve". The selected system's parameters are list in Table I.

Table I: Parameters of the system

Parameter	Symbol	Value
Grid phase voltage	v_{abc}	$220V_{rms}$
Grid frequency	f_o	50 Hz
PI controller and Hysteresis band	k_p, k_i and HB	0.1, 1, 2 (A)
Output voltage	V_o	$700V_{dc}$
DC-link inductor	L_{dc}	2 mH
DC-link Capacitor	C_{dc}	470 μF
Load	R_L	163 Ω
Grid Impedance	Z_g (L_g, R_g)	0.18 mH, 0.1 Ω

For the first case 7th and 13th and for the second case 5th and 13th harmonics were selected to be reduced. Therefore, k and m in (5) should be changed to the selected harmonic orders. Fig. 5 and Fig. 6 depicted the obtained results for the three-phase input currents. The simulated results illustrates that the applied modulation has significantly affected the desired harmonics. Table II summarized the obtained results in comparison with the conventional square wave method. It is to be noted that the conventional square-wave method is also known as one of the effective approaches [1-3, 6]. As can be seen the targeted harmonic components have not fully nullified. This is due to the presence of non-ideal parameters especially the grid impedance which slightly reduces the performance of the system.

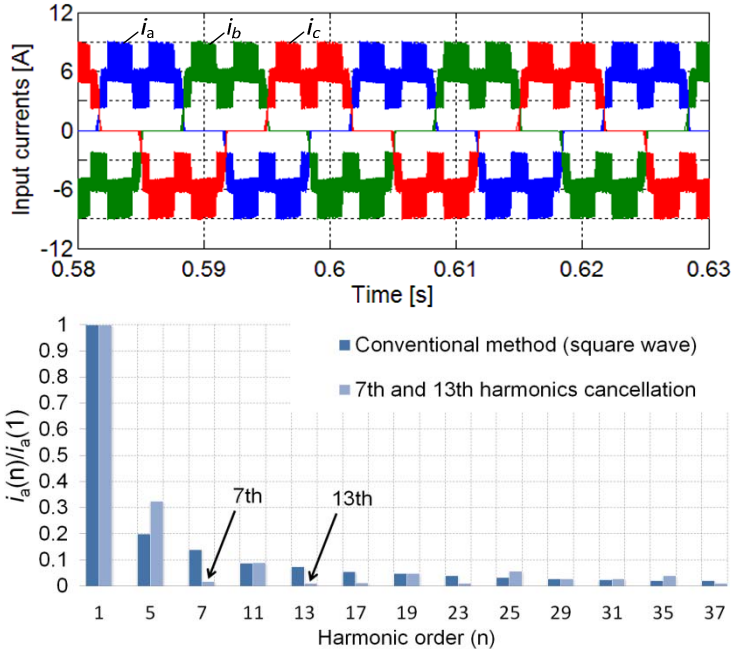
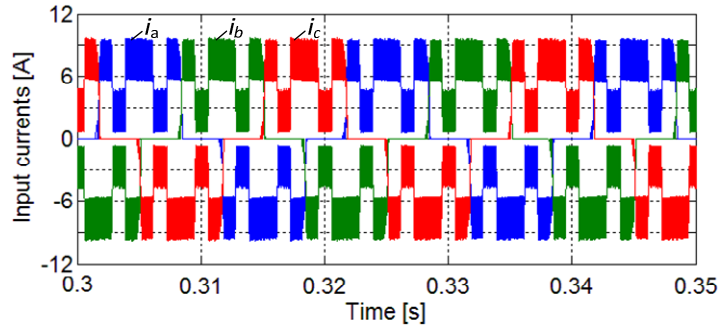


Fig. 5: Simulation results for 7th and 13th harmonics cancellation using hysteresis current control: (a) Two-level three-phase input currents, (b) input current (i_a) (Fast Fourier Transform) in comparison with conventional square-wave method [with $Idc_1 = 1$, $Idc_2 = 0.618$, $\alpha_1 = 42^o$].

(a)



(b)

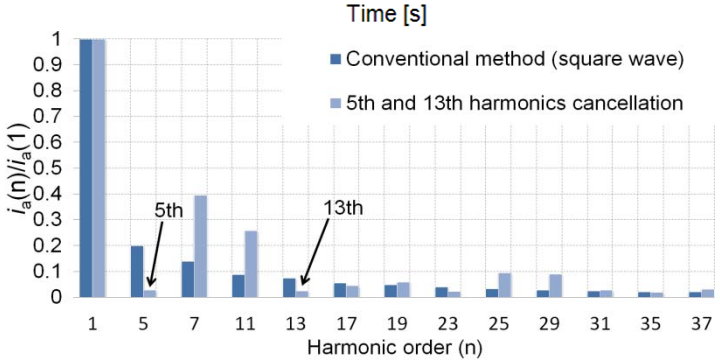


Fig. 6: Simulation results for 5th and 13th harmonics cancellation using hysteresis current control: (a) Two-level three-phase input currents, (b) input current (i_a) FFT in comparison with conventional square-wave method [with $Idc_1 = 1$, $Idc_2 = 0.653$, $\alpha_1 = 70^o$].

Table II: Harmonic distribution of simulation cases at a power level of 3 kW

Harmonic Mitigation Strategy	Harmonic Distribution and THD_i (%)				
	$i_a(5)/i_a(1)$	$i_a(7)/i_a(1)$	$i_a(11)/i_a(1)$	$i_a(13)/i_a(1)$	THD_i
7th and 13th harmonic cancellation	32.4	1.7	8.9	1	35
5th and 13th harmonic cancellation	2.8	39.5	25.8	2.4	49.9
Conventional method (square wave)	20	14	8.8	7.4	29

6. Experimental Results

In this section the experimental results of the implemented prototype (Fig. 4(b)) are presented. The system parameters have been set following Table I. The measured input currents along with the input current FFT (Fast Fourier Transform) for both considered cases in previous section are depicted in Fig. 7 and Fig. 8. The results show that the proposed method effectively attenuates desired harmonics. Table III compares experimental results based on the proposed and conventional methods. Same as in simulations, due to the presence of line impedance, the targeted harmonic components have not fully nullified. Accounting the grid impedance in (5) can resolve this issue. However, in reality, the grid impedance is unknown and a real-time calculation of the grid-impedance should be applied to the proposed modulation method.

Results obtained at simulation and experimental levels show that up to two low order harmonics can be cancelled out applying the proposed current modulation technique. However, this does not hold true for 5th and 7th harmonics. In fact, as can be seen from Table II and III reducing 5th harmonic increases 7th harmonic and vice versa, which results in higher THD_i comparing with the conventional case. This can be understood by solving (5) for these harmonic orders. The solution for eliminating 5th harmonic requires to select $60^o<\alpha_1<90^o$ which is contrary to 7th harmonic where $34^o<\alpha_1<60^o$ making it impossible to target these two harmonics at the same time. The possible solutions have been briefly addressed in the next section as the future development.

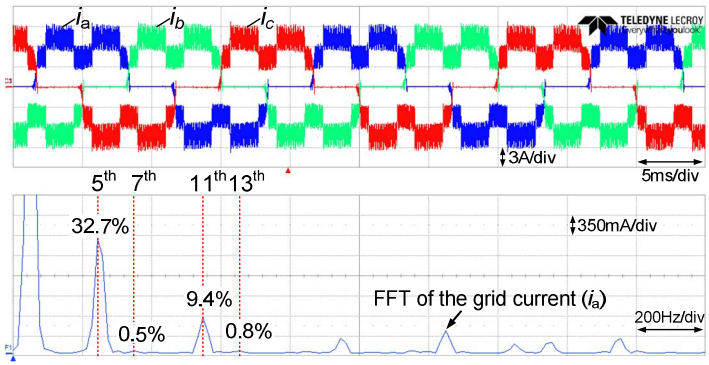


Fig. 7: Experimental results for 7th and 13th harmonics cancellation using hysteresis current control at V_o = 700V_{dc} and P_o ≈ 3kW: (a) Two-level three-phase input currents, (b) input current (i_a) FFT [with Idc_1 = 1, Idc_2 = 0.618, α_1= 42°].

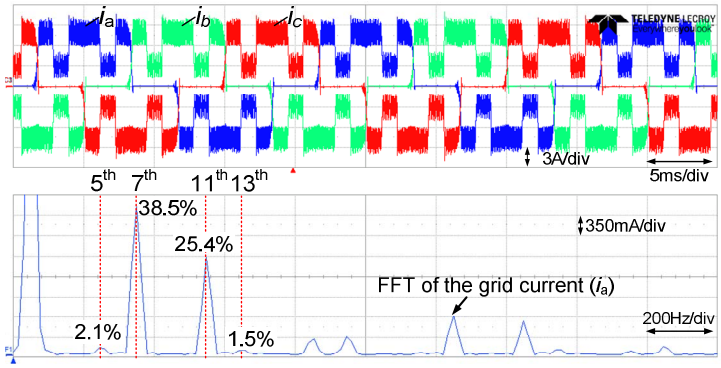


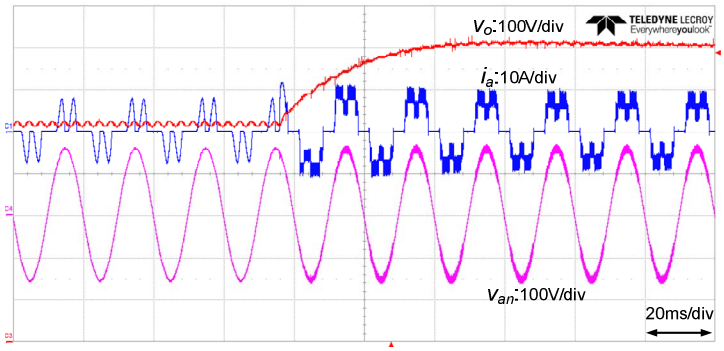
Fig. 8: Experimental results for 5th and 13th harmonics cancellation using hysteresis current control at V_o = 700V_{dc} and P_o ≈ 3kW: (a) Two-level three-phase input currents, (b) input current (i_a) FFT [with Idc_1 = 1, Idc_2 = 0.653, α_1= 70°].

Table III: Harmonic distribution of practical cases at a power level of 3 kW

Harmonic Mitigation Strategy	Harmonic Distribution and THD_i (%)				
	$i_a(5)/\ i_a(1)$	$i_a(7)/\ i_a(1)$	$i_a(11)/\ i_a(1)$	$i_a(13)/\ i_a(1)$	THD_i
7th and 13th harmonic cancellation	32.7	0.5	9.4	0.8	35.5
5th and 13th harmonic cancellation	2.1	38.5	25.4	1.5	48.6
Conventional method (square wave)	20.8	13.1	8.8	7	29

Finally, the start-up and shut-down dynamic behavior of the implemented system are illustrated in Fig. 9. For the start-up case the input voltage is already applied, the load current is flowing and boost converter is in off state. Turning on the dc-dc converter makes the controller to starts the pulse pattern modulation at input current i_a and changes the output voltage V_o from 515V_{dc} to 700V_{dc} without any large overshoot (Fig. 9(a)). The symmetrical pulse patterns on the input current after 100ms validate the PLL settling time. At shut-down phase of operation the control circuit permanently turns off the IGBT switch so that it stops current modulation and the output voltage drops to 515V_{dc} (Fig. 9(b)).

(a)



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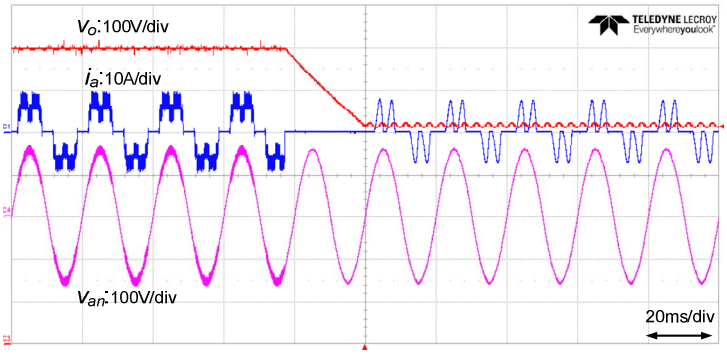

Fig. 9: Measured dynamic behavior of input current i_a and output voltage V_o at (a) startup and (b) shutdown at the nominal operating conditions.

7. Future Development

The proposed concept gives the possibility to eliminate up to two low order harmonics in a three-phase diode bridge rectifier based on electronic inductance topology. Therefore, based on the application requirement employing the proposed method can further improve the input current quality by reducing low order harmonics. However, as stated before, targeting 5^{th} and 7^{th} harmonic orders simultaneously solely based on a single unit system is impossible. In this section, possible solutions are briefly discussed which emphasis on the advantage of employing the proposed approach.

The first solution is based on employing a shunt passive trap filter [10] tuned at 5^{th} or 7^{th} harmonic in conjunction with the proposed method. According to the obtained results in Fig. 7 and Fig. 8, 5^{th} harmonic order can be reduced with the cost of increasing 7^{th} harmonic order and vice versa. Therefore, placing a trap filter tuned at the elevated harmonic order can significantly improve the THD_i and input current quality. In practice, in order to have a smaller size filter, applying a trap filter at 7^{th} harmonic is preferred rather than having a trap filter tuned at 5^{th} harmonic order.

Secondly, the proposed method can be applied to multi-pulse rectifier systems [11] or combination of nonlinear loads [19]. Fig. 10(a) illustrates the application of the proposed concept in a 12-pulse rectifier topology with a common dc-bus. Basically, the 12-pulse arrangement eliminates the 5^{th} and 7^{th} harmonic orders. Hence, employing the proposed current modulation strategy can further improve the input current quality by targeting 11^{th} and 13^{th} harmonic orders. The obtained results in Fig. 10(b) and Fig. 10(c) show that the new 12-pulse system obtained $THD_i \approx 6\%$, while the conventional 12-pulse rectifier harmonic distortion depending on the output power level varies between $10\% < THD_i < 15\%$. Therefore, employing the new 12-pulse system shown in Fig. 10 has a same performance as in a conventional 18-pulse rectifier system. In addition, the output voltage can be increased to higher voltage levels using the boost topology; this is beneficial when the dc-link voltage is fed to an inverter. Moreover, unlike the conventional multi-pulse rectifier systems which the performance of the system is dependent of the load profile, applying the proposed concept can maintain the input current THD_i regardless of the output power variation.

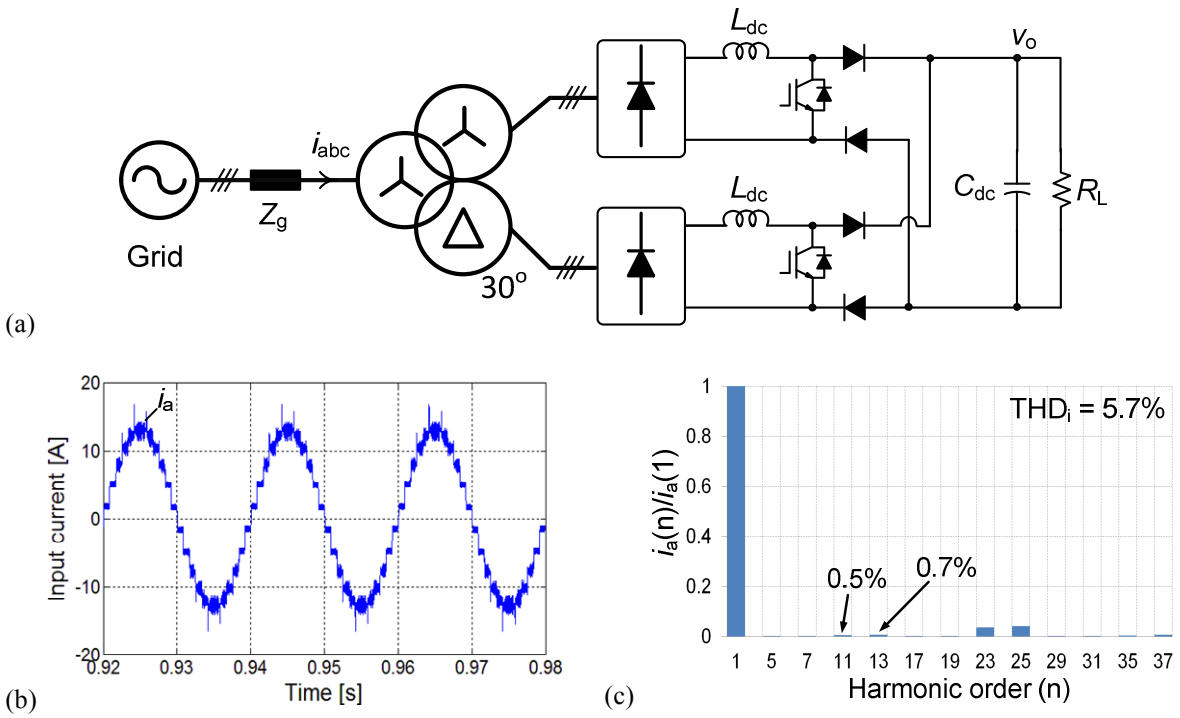

Fig. 10: Extension of conventional 12-pulse rectifier system based on proposed current modulation strategy: (a) circuit schematic, (b) simulated input current waveform (i_a) and (c) input current FFT at $V_o = 700V_{dc}$ and at $P_o = 6kW$.

8. Conclusions

In this paper a novel current modulation technique has been proposed for a three-phase rectifier with an electronic inductor at the dc-link side. The proposed method modulates the dc-link current to control the fundamental current and to cancel selected line current harmonics by adding or subtracting phase-displaced current levels. Due to different variables defined in the current modulation scheme, an optimum current waveform can be developed to reduce or cancel low order harmonics. A main advantage of the proposed method is that the relative values of harmonics with respect to the fundamental value remain constant regardless of load profile variation. Moreover, the flexibility of the proposed concept has been discussed in conjunction with multi-pulse systems in order to further improve the input current quality.

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